

# FLY HEIGHT CONTROL FOR A READ/WRITE HEAD IN A HARD DISK DRIVE

\* \* \* \* \*

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] Not applicable.

## STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] Not applicable.

## BACKGROUND OF THE INVENTION

[0003] This invention is in the field of disk drive control circuits, and is more specifically directed to a preamplifier for a read/write head in a hard disk drive.

[0004] Continuing progress toward higher performance yet less expensive  
5 personal computers, including both desktop workstations and portable computers, has  
resulted in large part from advances in nonvolatile data storage technology. As is well  
known in the art, the capacity of conventional disk drives has greatly increased over  
recent years, at ever decreasing cost per megabit. This capacity increase is directly  
related to improvements in the density with which data can be stored in a magnetic disk  
10 drive, particularly in "hard" disk drives (i.e., disk drives in which the magnetic disk is  
not removable from the location of the read/write heads). Advances in disk drive  
technology have decreased the surface area required to reliably and retrievably store a  
bit along a "track" on the disk surface, and have also decreased the spacing between  
adjacent tracks. This reduction in the active disk surface area per unit of storage has  
15 been enabled, in large part, by corresponding reductions in the size and precision of the  
magnetic transducers, commonly referred to as "heads", that effect the writing and  
reading operations in magnetic disk drives.

[0005] In conventional magnetic disk drives, the writing and reading of stored data is carried out by way of near-field magnetic processes. To write data, ferromagnetic domains at the disk surface are selectively oriented by applying a magnetic field in close proximity to the disk surface. One type of conventional write head is the well-known inductive writer, which includes an electromagnet having a gap that can be positioned near the magnetic disk surface. The electromagnet is selectively energized to establish a magnetic field, at the gap, that is strong enough to define a magnetic "transition pattern" of the desired polarity at the addressed location of the disk surface. Data is read from the disk by sensing the polarity of the magnetic field established by these magnetic transition patterns. Conventional read heads include inductive heads consisting of an electromagnet (which may be the same electromagnet used to write data) in which a current is induced by the magnetic fields at the disk surface; more recently, read heads are implemented by a magnetoresistive (MR) head having a resistance that varies with the polarity of the magnetic field.

[0006] In modern disk drives, the read/write heads are disposed within a "slider" at the distal end of a head gimbal assembly (HGA) suspension. The flexible HGA suspension is attached to an actuator, which includes a so-called "voice coil" motor that positions the heads at the desired locations of the disk surface. The relative motion between the spinning disk surface and the slider creates a lifting force on the slider, establishing an air bearing surface (ABS) on which the slider rides over the disk surface. Typically, the heads are located at the trailing edge of the slider, which is typically closer to the disk surface than is the slider leading edge.

[0007] In connection with these near-field mechanisms, the magnetic field strength varies exponentially as the distance between the magnetic transducers (read/write heads) and the magnetized disk surface shrinks. It has been observed that the areal density of data storage at the disk surface, for a given bit error rate (BER), depends strongly on the distance between the heads and the disk surface. The spacing maintained by the air bearing surface (ABS) between the read/write heads and the disk surface is referred to in the art as the "fly height" of the heads. In modern conventional

disk drives, the mean fly height is on the order of a few nanometers. Low fly heights have enabled the very high areal densities attained in modern disk drives.

[0008] However, low fly heights tend to increase the wear of both the disk surface and the read-write heads. At extremely low fly heights, relatively small  
5 asperities in the disk surface can cause contact between the slider and the disk surface, depleting and degrading lubricants, causing wear on both the slider and the disk surface and causing contamination from wear particles, and in some cases causing the heads to stick at locations of the disk surface where contact is made.

[0009] Disk drive manufacturers are thus faced with a tradeoff between disk  
10 drive reliability, on one hand, and areal density and BER, on the other hand, in determining the desired fly height of the read/write heads. Accordingly, significant effort has been and is being expended in the art to provide extremely smooth magnetic disk surfaces, so that very low fly heights can be achieved while still providing reasonable disk durability. By way of further background, active control of the fly  
15 height by way of a micromechanical air valve is described in U.S. Patent No. 6,578,816 B1.

[0010] It is also known that the writing current conducted by the inductive write head causes resistive heating at the read/write head, and in turn causes thermal expansion of the write head and, in some cases, also of the MR read head (or inductive  
20 read head, if present). This thermal expansion typically causes reduction in the fly height. But if the nominal fly height of the read/write head is already extremely small, this thermal expansion of the read/write head can cause contact between the disk surface and the read/write head, resulting in disk and head wear and in the degradation of the disk system described above.

[0011] By way of further background, it is known to include a resistor within the  
25 slider of a disk drive read/write head for controlling the fly height. An example of this construction is described in U.S. Patent No. 5,991,113. As described in this reference, the

application of a current to the resistor heats and thus expands the read/write heads, reducing the fly height of the read/write heads from the disk surface.

## BRIEF SUMMARY OF THE INVENTION

[0012] It is therefore an object of this invention to provide a control circuit and method for controlling the fly height of read/write heads in a disk drive.

5 [0013] It is a further object of this invention to provide such a control circuit and method that controls fly height by controlling current through a heating resistor at the heads.

[0014] It is a further object of this invention to provide such a control circuit and method that accounts for increased resistive heating in write cycles relative to read cycles.

10 [0015] Other objects and advantages of this invention will be apparent to those of ordinary skill in the art having reference to the following specification together with its drawings.

[0016] The present invention may be implemented into a preamplifier circuit for controlling current applied to a heat element resistor located near the read/write heads  
15 in a magnetic disk drive. The circuit includes a driver that supplies the current to the heat element resistor according to separate programmable levels for read and write operations. The circuit also includes sensing circuitry for optimizing the fly height during operation.

[0017] According to another aspect of the invention, the preamplifier circuit  
20 includes programmable underdrive and overdrive functionality, for driving the heat element resistor during transitions between reads and writes. According to another aspect of the invention, the circuit is adaptable to independently control the fly height of multiple read/write heads, in a multiple platter disk drive.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0018] Figure 1 is an electrical diagram, in block form, of a computer system including a hard disk drive subsystem and control circuitry, constructed according to the preferred embodiment of the invention.

5 [0019] Figure 2 is a plan view illustrating the construction of a portion of the hard disk drive in the system of Figure 1.

[0020] Figure 3 is a cross-sectional view illustrating the construction of a read/write head assembly in the system of Figure 1.

10 [0021] Figure 4 is an electrical diagram, in schematic form, illustrating the construction of control circuitry for controlling a heat element resistor in the read/write head assembly, according to a first preferred embodiment of the invention.

[0022] Figure 5 is an electrical diagram, in schematic form, illustrating the construction of control circuitry for controlling a heat element resistor in multiple read/write head assemblies of a disk drive subsystem, according to a second preferred  
15 embodiment of the invention

[0023] Figure 6 is a timing diagram, illustrating the operation of the control circuitry of Figure 5 according to the second preferred embodiment of the invention

## DETAILED DESCRIPTION OF THE INVENTION

[0024] The present invention will be described in connection with its preferred embodiment, namely as implemented into a magnetic disk drive using an inductive write head and a magnetoresistive (MR) read head disposed in a slider having a heat element resistor. It is believed that this invention is especially beneficial in such an application. However, it will be appreciated that this invention may also be implemented in, and provide significant benefit to, disk drives of other types and construction, including disk drives utilizing different read and write head technology and mechanisms. Accordingly, it is to be understood that the following description is provided by way of example only, and is not intended to limit the true scope of this invention as claimed.

[0025] Figure 1 illustrates an exemplary example of a computer system into which the preferred embodiment of the invention is implemented. In this example, personal computer or workstation 2 is realized in the conventional manner, including the appropriate central processing unit (CPU), random access memory (RAM), video and sound cards or functionality, network interface capability, and the like. Also contained within computer 2 is host adapter 3, which connects on one side to the system bus of computer 2, and on the other side to bus B, to which disk drive controller 5 is connected. Bus B is preferably implemented according to conventional standards, examples of which include the Enhanced Integrated Drive Electronics (EIDE) standard or the Small Computer System Interface (SCSI) standard. Other disk storage devices (hard disk controllers, floppy drive controllers, etc.) and other peripherals may also be connected to bus B, as desired and in the conventional manner.

[0026] Controller 5 is a conventional disk drive controller as known in the art. In modern disk drives in which the drive electronics is implemented at the disk drive rather than as a controller at computer 2 itself, controller 5 is implemented in a printed circuit board within the disk drive itself. Of course, in larger scale systems, controller 5 may be implemented within computer 2. In the generalized block diagram of Figure 1,

the components of controller 5 are shown according to their functions, rather than their physical integrated circuits, for the sake of clarity. Typical integrated circuits used to implement disk drive controllers such as controller 5 include a digital signal processor (DSP), read-only memory (ROM) and random access memory (RAM), other non-volatile storage such as flash RAM, interface circuitry connected to bus B, and other custom logic circuitry. Functionally, controller 5 includes data channel 4, which is interfaced with bus B and effects the function of communicating data to and from preamplifier 10 at head-disk assembly 20. Data channel 4 is also in communication with servo control 6, which may also include a demodulation function. Servo control 6 in turn communicates with motion and power controller 8, which drives voice coil motor 12 and spindle motor 14 in head-disk assembly 20.

[0027] Head-disk assembly 20 includes the electronic and mechanical components that are involved in the writing and reading of magnetically stored data. In this example, head-disk assembly 20 includes one or more disks 18 having ferromagnetic surfaces (preferably on both sides) that spin about their axis under the control of spindle motor 14. Multiple read/write head assemblies 15a, 15b are movable by actuator 17. Accordingly, signals from motion and power control function 8 in controller 5 control spindle motor 14 and voice coil motor 12 so that actuator 17 places the read/write head assemblies 15a, 15b at the desired locations of disk surface 18 to write or read the desired data.

[0028] Figure 2 illustrates, in further detail, the physical arrangement of disk surface 18 relative to its associated read/write head assembly 15. Disk surface 18 is shown, in this example, as rotating in a primary direction (counterclockwise, in this example) about its axis; as known in the art, this rotation is effected by spindle motor 14 under the control of controller 5. As shown in Figure 2, read/write head assembly 15 is disposed at the end of actuator arm 22, which is rotatable (about its axis, not shown) by actuator 17 as effected by voice coil motor 12. Rotation of actuator arm 22 will position read/write head assembly 15 at the appropriate radial distance of disk surface 18 to access the desired track.



[0029] Figure 3 illustrates the construction of read/write head assembly 15 according to the preferred embodiment of this invention. Read/write head assembly 15 includes slider 21, which is typically a ceramic, silicon, or other electrically insulating body into which read head 25R and write head 25W may be formed. The size and shape of slider 21 is designed to provide an air bearing surface (ABS) between it and rotating disk surface 18. Slider 21 is mounted to actuator arm 22 in the conventional manner.

[0030] Read head 25R and write head 25W are disposed near the trailing edge of slider 21, defined by the rotation of disk surface 18 (see Figure 2). The particular construction and implementation of read and write heads 25R, 25W may vary, according to the desired disk drive performance. In this embodiment of the invention, write head 25W is preferably implemented as an inductive write head, including an electromagnet formed with windings about an iron core having a gap oriented toward the bottom of slider 21, to direct the field generated by a current through the windings toward the nearby disk surface 18. Read head 25R is preferably constructed as a magnetoresistive (MR) or giant magnetoresistive (GMR) material. For example, as known in the art, a GMR element is a "stripe" of a soft magnetic material, such as iron chromide (FeCr), which has a resistance value that varies with the polarity of a magnetic field applied to the element. Alternatively, read head 25R may also be implemented as an inductive read head, in which a current is induced into an electromagnet by the magnetic field of a portion of disk surface 18 moving nearby.

[0031] According to this embodiment of the invention, read/write head assembly 15 also includes heat element resistor 30, which is shown schematically in Figure 3. Heat element resistor 30 may be a conventional resistor of various construction (e.g., a carbon body resistor), or alternatively constructed as a resistance heater in the manner known in the art. Heat element resistor 30 is disposed within slider 21, at an appropriate position so that it can readily heat write head 25W (and read head 25R, if constructed as an inductive head). As known in the art, the fly height of a disk drive head is typically defined by the distance between the inductive heads and the disk surface, and that thermal expansion of the inductive core of the head or heads, for

example due to resistive heating by the current passing through the windings, ultimately defines this distance. According to this preferred embodiment of the invention, preamplifier and fly height controller 10 controls the current through heat element resistor 30, and thus controls the fly height of read/write head assembly 15, as will now be described relative to Figure 4.

[0032] Figure 4 illustrates the construction of fly height controller 10FHC, which is a portion of preamplifier and fly height controller 10 in the system of Figure 1. The portion of preamplifier and fly height controller 10 of Figure 1 that is in the data path between controller 2 and read/write heads 15 is not shown in Figure 4 for the sake of clarity; that data path portion of preamplifier and fly height controller 10 may be realized in the conventional manner. As shown in Figure 4, fly height controller 10FHC drives resistor 30 from pad PAD. In this regard, preamplifier and fly height controller 10 is contemplated as being implemented by way of an integrated circuit, with pad PAD connected by a wire bond or otherwise to an external terminal of the integrated circuit, to which heat element resistor 30 is connected. Of course, those skilled in the art having reference to this specification will recognize that portions of preamplifier and fly height controller 10 may be instead realized by way of more than one integrated circuit or discrete components, or integrated into a larger scale integrated circuit. More specifically, it is contemplated that fly height controller 10FHC may be implemented in a separate integrated circuit from the data path portion of preamplifier and fly height controller 10.

[0033] As will become apparent from the following description, fly height controller 10FHC effects fly height control differently during disk read operations than during disk write operations. This separate read and write fly height control accounts for the relatively high current that is supplied to write head 35W, as compared with the relatively low read current applied to read head 35R if implemented as an MR head, or the relatively low read current induced into an inductive read head 35R. This higher write current has been observed to resistively heat write head 35W, causing it to thermally expand and reduce the fly height during write operations; conversely, the

lower current levels applied or induced during read operations reduce the resistive heating and cause write head 35W to thermally contract, increasing the fly height during read operations. According to the preferred embodiment of the invention, therefore, the current applied to heat element resistor 30 is preferably higher during read operations than during write operations, to balance the relative current levels through the active heads 35W, 35R.

[0034] As shown in Figure 4, fly height controller 10FHC includes read current register 32R and write current register 32W, each of which receive and store digital control signals, preferably from controller 5, that indicate the desired current levels to be applied to heat element resistor 30 during read and write operations, respectively. According to the preferred embodiment of this invention, as will be described below, fly height controller 10FHC applies different current levels for transitions between read and write operations, and as such the desired current level signals received by registers 32R, 32W correspond to the desired heat element resistor 30 currents during steady-state read and write operations, respectively.

[0035] Registers 32R, 32W apply their outputs to inputs of multiplexer 34, the output of which is applied to steady-state digital-to-analog converter (DAC) 36. Multiplexer 34 receives a control input from fly height control (FHC) logic 35, responsive to which multiplexer 34 selects the appropriate register 32R, 32W contents for application to steady-state DAC 36 in read and write operations, respectively. FHC logic 35 receives various control signals, for example from controller 5, including control signal RXW that indicates whether a read or write operation is active, control signal HDSEL that indicates selection of the read/write head assembly 15 associated with heat element resistor 30 being controlled by fly height controller 10FHC, and control signal FHC\_EN that enables the operation of fly height controller 10FHC itself. An output of FHC logic 35 is applied as a control signal to multiplexer 34, to select the output of read current register 32R in read operations, and to select the output of write current register 32W in write operations (assuming that control signals HDSEL, FHC\_EN indicate selection of this read/write head assembly 15 and enabling of fly height control).

[0036] The analog output of steady-state DAC 36 is applied to the input of voltage driver 40. Voltage driver 40 is an amplifier that drives a voltage at its output responsive to the voltage at its input from steady-state DAC 36. The gain of voltage driver 40 is preferably greater than unity, for example on the order of two, to facilitate amplifier design and preserve headroom. The output of voltage driver 40 is connected, via switch 41, to pad PAD and thus to heat element resistor 30 connected to pad PAD. Accordingly, in normal operation (with switch 40 closed to connect voltage driver 40 to pad PAD), voltage driver 40 drives heat element resistor 30 responsive to the analog output of steady-state DAC 36, which in turn corresponds to the appropriate steady-state digital signal stored by read current register 32R and write current register 32W, corresponding to the current read or write operation.

[0037] Real time monitoring of the power delivered to heat element resistor 30 is also provided in fly height controller 30, according to the preferred embodiment of the invention. The output of voltage driver 40 is also applied to current mirror 42, which is constructed in the conventional manner for current mirror circuits. Current mirror 42 and series resistor 49A define a path between the  $V_{cc}$  power supply and ground. In this manner, current mirror 42 conducts a current, through resistor 49A, that corresponds to (i.e., "mirrors") the current through heat element resistor 30. The voltage across resistor 49A is applied to one input of comparator 47. A second input of comparator 47 receives the voltage across resistor 49B, which is connected between the analog output of BHV DAC 46 and ground. The output of comparator 47 corresponds to a fault signal, and is forwarded to FHC logic 35 and to fault logic elsewhere, such as in controller 5. In a measurement mode, the output voltage of BHV DAC 46 can be programmed, for example by controller 5, to match the mirrored current (when comparator 47 asserts the fault signal), at which point the programmed voltage provides a measure of the resistance of heat element resistor 30 and the power delivered to it by voltage driver 40. Conversely, during normal read and write operations, BHV DAC 46 preferably receives a control signal, for example from controller 5, corresponding to a "safe" level of current through heat element resistor 30. In this normal mode, comparator 47 will issue a fault

signal if the mirrored current corresponding to the output of voltage driver 40 exceeds this safe level, responsive to which FHC logic 35 preferably disables voltage driver 40 to protect read head 35R and write head 35W. This operation is particularly useful in ensuring that the overdrive of heat element resistor 30 (between write and read  
5 operations, as described below) does not damage read and write heads 35R, 35W.

[0038] According to this embodiment of the invention, fly height controller 10FHC also includes circuitry for adjusting the current through heat element resistor 30 during transitions between read and write disk operations. These adjustments are applied in the form of relatively brief overdrive (high current to heat element resistor 30)  
10 and underdrive (low current to heat element resistor 30) pulses, each of which assist in the settling of the steady-state temperature of heads 35R, 35W for the ensuing operation. More specifically, during a transition from a read operation to a write operation, it is preferred to briefly underdrive heat element resistor 30, removing the active drive current of heat element resistor 30 prior to the higher current becoming applied through  
15 write head 35W, and the resulting heating of write head 35W, in the write operation. Conversely, during a transition from a write operation to a read operation, it is preferred to briefly overdrive heat element resistor 30, to more rapidly bring read head 35R to temperature for the read operation. The duration of the overdrive and underdrive pulses may be programmed by way of a timer, or alternatively may be manually  
20 controlled via a serial interface to fly height controller 10FHC.

[0039] In this embodiment of the invention, current source 38 applies a fixed current to its associated capacitor 38C, which has its top plate connected to an input of comparator 43 and its bottom plate at ground. Overdrive time register 39 receives a programmable value, for example from controller 5, corresponding to the desired  
25 duration of the overdrive and underdrive pulses, and applies an output signal to associated resistor 39R to define a control voltage to a second input of comparator 43. The fixed current from current source 38 to capacitor 38C generates a ramped voltage across capacitor 38C, which is compared against the voltage from overdrive time register 39 by comparator 43. Accordingly, comparator 43 generates a pulse at its

output, which is applied to FHC logic 35, having a duration corresponding to the time that the ramped voltage at capacitor 38C is below the programmed voltage from overdrive time register 39. This pulse duration from comparator 43 is used to set the duration of the overdrive and underdrive pulses, as controlled by FHC logic 35.

5    [0040]        In response to transitions between read and write operations, and to the disabling and enabling of the selected head (as indicated by control signal HDSEL), FHC logic 35 issues control signals on control line OD\_L to the gate of p-channel metal-oxide-semiconductor (MOS) transistor 44P, and on control line UD to the gate of n-channel MOS transistor 44N. Transistors 44P, 44N have their source/drain paths connected in  
10    series between the  $V_{cc}$  power supply and ground. The node at the drains of transistors 44P, 44N is connected to the input of voltage driver 40, and at pull-down resistor 36R. Transistors 44P, 44N are preferably sized to be capable of overriding the output signal from steady-state DAC 36.

15    [0041]        In steady-state operation, FHC logic 35 issues inactive levels on control lines OD\_L and UD (inactive levels being high and low logic levels, respectively), to keep transistors 44P, 44N both in an off state. Responsive to a transition from a write operation to a read operation, as indicated by a change of state of control signal RXW, FHC logic 35 issues an active (low logic level) pulse on control line OD\_L to the gate of transistor 44P, maintaining an inactive (low level) signal on control line UD. As  
20    mentioned above, the duration of the active pulse on control line OD\_L is determined by comparator 43, in response to the programmed duration in overdrive time register 39. This active pulse on control line OD\_L turns on transistor 44P (transistor 44N remaining off), which drives the input of voltage driver 40 to a high voltage near or at the  $V_{cc}$  power supply. This causes voltage driver 40 to apply a high voltage to heat element  
25    resistor 30 for the duration of the pulse, if monitoring comparator 47 does not issue an fault signal due to excessive drive before that time, as mentioned above.

[0042]        Conversely, responsive to a transition from a read operation to a write operation, FHC logic issues an active (high level) pulse on control line UD and

maintains an inactive (high level) on control line OD\_L. The duration of this pulse is also determined by comparator 43, in response to the programmed duration in overdrive time register 39. During this pulse, transistor 44N is turned on while transistor 44P remains off, pulling the input to voltage driver 40 toward ground. This  
5 reduces the voltage applied to heat element resistor 30 by voltage driver 40, and thus the current through heat element resistor 30, for the duration of this underdrive pulse.

[0043] Also according to the preferred embodiment of the invention, fly height controller 10FHC also includes optional circuitry for establishing an initial state of current through heat element resistor 30. This initial state corresponds to the current to  
10 be applied to heat element resistor 30 during such time as its associated read/write head assembly 15 is not selected. Preferably, the initial state current applied to heat element resistor 30 is selected so that the switching time is minimized when its read/write head assembly 15 is selected, and also to minimize power dissipation at unselected read/write heads, as is especially important in portable computing devices.

15 [0044] In fly height controller 10FHC, initial state register 50 receives a digital value, for example from controller 5, that indicates the desired level of current to be applied to heat element resistor 30 during initial state time intervals, such as when the read/write head assembly 15 associated with heat element resistor 30 is not selected. This digital value stored in register 50 is applied to an input of initial state DAC 52,  
20 along with control signal IC\_EN, which indicates that the initial state current level feature of fly height controller 10FHC is to be enabled. When enabled by control signal IC\_EN, initial state DAC 52 generates an analog signal corresponding to the digital value from initial state register 50, and applies this analog signal to initial state voltage driver 54, which is a conventional amplifier circuit for generating a corresponding  
25 output signal that produces the desired initial state current through heat element resistor 30. Initial state voltage driver 54 may be biased to a different power supply voltage (e.g., VCC\_FHC) from that biasing steady-state voltage driver 40, if desired. For example, the bias voltage VCC\_FHC applied to initial state voltage driver 54 may be a lower power supply voltage, to save power. The output of initial state voltage driver 54

is connected to one pole of control switch 41; the other pole of control switch 41 in this embodiment of the invention is connected to the output of main voltage driver 40, described above. The throw of control switch 41 is connected to pad PAD, and thus to heat element resistor. Control switch 41 may be implemented in the conventional  
5 manner for integrated circuits, such as by way of MOS pass transistors in the case where fly height controller 10FHC is implemented in MOS technology.

[0045] In the operation of this initial state feature, FHC logic 35 controls the state of control switch 41 according to whether the read/write head assembly 15 containing heat element resistor 30 is selected. As mentioned above, this selection is indicated by  
10 control signal HDSEL, which is applied by controller 5 in this example. If read/write head assembly 15 is not selected, FHC logic 35 issues the appropriate signal to control switch 41 to connect the output of initial state voltage driver 54 to pad PAD. If the initial state function is enabled (by control signal IC\_EN), a voltage corresponding to the digital value in initial state register 50 is applied to heat element resistor 30. Conversely,  
15 if read/write head assembly 15 is selected, FHC logic 35 places control switch 41 in its position that connects the output of main voltage driver 40 to pad PAD, so that the voltage indicated by steady-state DAC 36 is applied to pad PAD, and thus to heat element resistor 30.

[0046] As mentioned above, many modern disk drives include multiple disk  
20 surfaces, and correspondingly multiple read/write head assemblies. It may be desirable and beneficial in such disk drives to maintain unselected read/write head assemblies in an initial state from which transition to a read operation can be facilitated. In this regard, a separate fly height controller 10FHC may be provided for each read/write head assembly in each disk drive.

25 [0047] It is contemplated, however, that the provision of a separate fly height controller for each read/write head assembly may result in excessive power dissipation in some cases, especially for high capacity hard disk drives in portable computing equipment such as laptop personal computers. It has been observed, in connection with



another aspect of the invention, that the rate at which fly height control is effected is relatively slow, as compared with the switching time of modern digital logic circuitry. According to a second preferred embodiment of the invention, therefore, a multiple-head fly-height controller provides control of the fly height of multiple read/write head assemblies in a multiplexed manner.

[0048] Referring now to Figure 5, the construction of multiple-channel fly height controller 10FHC' according to this second preferred embodiment of the invention will now be described. According to this embodiment of the invention, a single instance of many of the components of fly height controller 10FHC described above can support fly height control for multiple read/write head assemblies 15, while separate voltage drive circuits 50<sub>0</sub> through 50<sub>n</sub> are provided for heat element resistors 30<sub>0</sub> through 30<sub>n</sub> in each of the multiple read/write head assemblies.

[0049] As shown in Figure 5, voltage drive circuit 50<sub>0</sub> includes steady-state voltage driver 40, initial state voltage driver 54, and control switch 41, all constructed and operating in the similar manner as described above relative to Figure 4. The other voltage drive circuits 50<sub>1</sub> through 50<sub>n</sub> are preferably similarly constructed. Accordingly, each voltage drive circuit 50 receives three control inputs, one being a steady-state voltage drive control signal applied to steady-state voltage driver 40, one being an initial state control signal applied to initial state voltage driver 54, and one being a control signal applied to control switch 41 to select which voltage driver output to be forwarded to its corresponding pad PAD and heat element resistor 30.

[0050] According to this embodiment of the invention, these control inputs applied to each voltage drive circuit 50 are generated from shared instances of many components in fly height controller 10FHC'. To the extent that these components are effectively identical to those in fly height controller 10FHC described above, these will be referred to in Figure 5 by the same reference numerals as used in Figure 4. In this implementation, steady-state DAC 36 and its input sources of read and write current registers 32R, 32W, and multiplexer 34, provide the steady-state read and write control

voltages for all of voltage drive circuits 50. Similarly, initial state DAC 52 and initial state register 50 provides the initial state control voltage for all of voltage drive circuits 50. Overdrive transistor 44P and underdrive transistor 44N provide overdrive and underdrive voltages for all of voltage drive circuits 50 in this embodiment of the invention, while comparator 43 provides the overdrive and underdrive pulse width timing for all of voltage drive circuits 50.

[0051] The ability to control multiple heat element resistors  $30_0$  through  $30_n$  according to this embodiment of the invention is provided by demultiplexer 60 and modified FHC logic 35'. In addition to the previously described inputs, FHC logic 35' also receives, in this embodiment of the invention, a multiple-bit digital signal on lines HEAD\_SEL that indicates which of the read/write head assemblies 15 (if any) is activated for a read or write operation. FHC logic 35' issues control signals to switches  $41_0$  through  $41_n$  in voltage drive circuits  $50_0$  through  $50_n$ , respectively, to select the appropriate one of steady-state voltage driver 40 or initial state voltage driver 54 in each of voltage drive circuits  $50_0$  through  $50_n$  according to the signal on lines HEAD\_SEL. In addition, according to this embodiment of the invention, FHC logic 35' includes timing logic for generating the select control signals that are applied to demultiplexer 60. Demultiplexer 60 receives the voltage control signals from the output of steady-state DAC 36 and from the output of initial state DAC 52, and applies these voltage control signals in a time-multiplexed fashion to voltage drive circuits  $50_0$  through  $50_n$ , under the timing control of FHC logic 35'. It is contemplated that the response of voltage drive circuits  $50_0$  through  $50_n$  and of heat element resistors  $30_0$  through  $30_n$  is sufficiently slow, relative to the switching capability of demultiplexer 60, that this time-multiplexed control of the application of the voltage control signals will adequately maintain fly height control for each of the multiple read/write head assemblies 15.

[0052] Also according to this embodiment of the invention, monitoring logic 51 also preferably monitors the voltages at each of pads  $PAD_0$  through  $PAD_n$  in a time-multiplexed fashion. In this exemplary implementation, a dedicated current mirror  $42_0$  through  $42_n$  is provided at the output of each of voltage drive circuits  $50_0$  through  $50_n$ ,

for providing a mirrored current to monitoring logic 51. Monitoring logic 51 is preferably constructed in the manner described above, for example including a BHV DAC for generating one or more reference levels, and a comparator for comparing a voltage derived from the mirrored current against the reference levels, along with the appropriate multiplexing circuitry for selecting the mirrored current to be monitored. As before, monitoring logic 51 preferably generates output signals that are applied to FHC logic 35' and to fault logic in controller 5.

[0053] According to this second preferred embodiment of the invention, the additional benefits of providing separate fly height control in each of multiple read/write head assemblies, while minimizing the power dissipation and circuit complexity required for such control by sharing the control logic and digital-to-analog converters among the multiple heads. In this way, the previously described advantages of programmable fly height control current for read and write operations, automatic programmable overdrive and underdrive levels for in transitions between read and write operations, and the inclusion of initial state drive level for the heat element resistor in unselected read/write heads, are provided for multiple heads in an efficient and cost-effective manner.

[0054] Referring now to Figure 6, an example of the operation of multi-channel fly height controller 10FHC' over a sequence of typical operational cycles will now be described. Of course, the particular sequence of operations encountered in practice will differ from that illustrated in Figure 6, and the particular current levels to be applied to heat element resistor 30<sub>0</sub>, 30<sub>1</sub> may differ from those relative levels indicated in Figure 6. It is contemplated that those skilled in the art having reference to this specification will readily comprehend, from this exemplary description, both how the preferred embodiment of the invention operates and also various alternative implementations for specific applications. The particular example illustrated in Figure 6 shows the fly height control operation for the case of two hard disk drive heads (HD0 and HD1) within a single disk drive 20, for which the fly height is controlled by associated heat element resistors 30<sub>0</sub>, 30<sub>1</sub>. It is contemplated that those skilled in the art, having reference to this

specification, will readily comprehend the operation of single-channel fly height controller 10FHC of Figure 4, as well as the operation of multi-channel fly height controller 10FHC' for more than two channels, from this description of the operation of multi-channel fly height controller 10FHC' for two channels.

5 [0055] At the beginning of this exemplary time sequence, shown at time  $t_0$  in the timing diagram of Figure 6, a read operation is being carried out using head HD0. As such, control signal RXW is at a high logic level, indicating that a read is being requested, and control signal HEAD\_SEL is at the appropriate state to select head HD0 (e.g., a high logic level applied to head HD0 and a low logic level to head HD1 as well as  
10 any other heads in the same hard drive 20, or alternatively by way of an encoded digital word that is decodable by each of heads HD0, HD1). As a result, with reference to Figure 4 by way of example, fly height controller 10FHC' is applying the digital word stored in read current register 32R to steady-state DAC 36, via multiplexer 34, and an analog signal from steady-state DAC 36 is applied to voltage driver 40. Because head  
15 HD0 is selected, FHC logic 35' in fly height controller 10FHC' controls demultiplexer 60 to apply the output of steady-state DAC 36 to voltage drive circuit 50<sub>0</sub>, within which control switch 41<sub>0</sub> selects the output of voltage driver 40<sub>0</sub> for application to pad PAD<sub>0</sub>, and thus to the heat element resistor 30<sub>0</sub> associated with head HD0. This voltage output V<sub>0</sub>, for head HD0, at this time is shown as voltage level RSS (read steady-state),  
20 corresponding to the contents of read current register 32R. Monitoring of the current through heat element resistor 30<sub>0</sub> by way of current mirror 42<sub>0</sub> and monitoring logic 51 may be carried out as desired.

[0056] Also during this time, with an active initial state enable control signal IC\_EN, FHC logic 35 in fly height controller 10FHC' controls demultiplexer 60 to apply,  
25 in a time-multiplexed fashion, the output of initial state DAC 52 applies corresponding to the contents of initial state register 50 to initial state voltage driver 54<sub>1</sub> in voltage drive circuit 50<sub>1</sub>, associated with the unselected head HD1. Voltage drive circuit 50<sub>1</sub> has placed its control switch 41<sub>1</sub> in the position to connect the output of initial state voltage driver 54<sub>1</sub> to pad PAD<sub>1</sub>. . The desired voltage level IC is thus applied through control

switch 41<sub>1</sub> to pad PAD<sub>1</sub> and to heat element resistor 30<sub>1</sub>, as illustrated in Figure 6 by voltage V<sub>1</sub> for head HD<sub>1</sub>. This state continues until the selection of head HD<sub>1</sub> (at time t<sub>4</sub> in Figure 6). In this initial state, monitoring of the initial state current through heat element resistor 30<sub>1</sub> by way of current mirror 42<sub>1</sub> and monitoring logic 51 may be carried out as desired.

[0057] Referring back to the sequence for selected head HD<sub>0</sub>, control signal RXW makes a transition at time t<sub>1</sub> to initiate a write operation at head HD<sub>0</sub>. In response to this transition, FHC logic 35' operates to change the state of multiplexer 34 to now select the digital value from write current register 32W for application to steady-state DAC 36, based upon which the output voltage will switch to voltage level WSS. Meanwhile, also responsive to the transition of control signal RXW at time t<sub>1</sub>, FHC logic 35' issues an active (high) level on line UD to the gate of transistor 44N, for the duration indicated by comparator 43 in response to the voltage at capacitor 38C and overdrive time register 39, which applies a low voltage via demultiplexer 60 to the input of voltage driver 40<sub>0</sub>, overriding the output of steady-state DAC 36. For this duration, as shown in Figure 6 beginning from time t<sub>1</sub>, underdrive voltage UD is applied to pad PAD<sub>0</sub> and thus to heat element resistor 30<sub>0</sub> for the selected head HD<sub>0</sub>. Upon expiration of the underdrive pulse, transistor 44N turns off again, and the output of steady-state DAC 36 applies the write steady-state voltage WSS as the output voltage V<sub>0</sub> at pad PAD<sub>0</sub>. In this embodiment of the invention, write steady-state voltage WSS is lower than read steady-state voltage RSS, to balance the relatively higher current that is supplied to write head 25W (and the resulting higher level of resistive heating and thermal expansion of write head 25W). Underdrive voltage level UD assists in the settling of the temperature of head HD<sub>0</sub> upon this transition to a write operation.

[0058] At time t<sub>2</sub>, control signal RXW makes another transition, this time back to the high level indicating a read operation. According to the preferred embodiment of the invention, FHC logic 35' in fly height controller 10FHC' includes a delay stage that delays its response to a write-to-read transition for a selected (preferably programmable) time delay RXW2ODTM, prior to initiating its write operation functions. This delay

period prevents the overdrive and overheating of its read/write head assembly 15 that can occur from response to an extremely short read operation. Following the expiration of this time delay RXW2ODTM, at time  $t_3$ , since control signal RXW has remained high in this example, FHC logic 35' issues an active (low) level on control line OD\_L for the pulse duration indicated by comparator 43, turning on transistor 44P and applying a high voltage, via demultiplexer 60, to the input of voltage driver 40<sub>0</sub>, overriding the output of steady-state DAC 36 and resulting in overdrive voltage level OD being driven by voltage driver 40<sub>0</sub> through control switch 41<sub>0</sub> to heat element resistor 30<sub>0</sub>. Meanwhile, FHC logic 35' (after the expiration of time delay RXW2ODTM) controls multiplexer 34 to select the contents of read current register 32R for application to steady-state DAC 36. In response, voltage driver 40<sub>0</sub> outputs read steady-state voltage RSS to heat element resistor 30<sub>0</sub>, as shown in Figure 6.

[0059] In the example of Figure 6, head HD1 becomes selected at time  $t_4$ , at which time head HD0 is deselected, as indicated by control signals HEAD\_SEL. In response to this event, FHC logic 35' in fly height controller 10FHC controls demultiplexer 60 to apply the output of initial state DAC 52 to voltage drive circuit 50<sub>0</sub>, and to control voltage drive circuit 50<sub>0</sub> to cause its control switch 41<sub>0</sub> to select the output of initial state voltage driver 54<sub>0</sub> rather than its main voltage driver 40<sub>0</sub>, for application to pad PAD. This output voltage  $V_0$  thus corresponds to the analog output of initial state DAC 52, and appears at pad PAD<sub>0</sub> and heat element resistor 30<sub>0</sub> as initial state voltage IC, as shown in Figure 6 for head HD0.

[0060] Conversely, for head HD1, because a read operation is indicated by control signal RXW, fly height controller 10FHC initiates control for the read operation by first issuing an overdrive voltage OD for the desired duration, via demultiplexer 60 and voltage drive circuit 50<sub>1</sub>, and then settling its output  $V_1$  to read steady-state voltage RSS as shown. The operation of fly height controller 10FHC' continues for the read and write operations as illustrated in Figure 6, in similar manner as described above for the case of selected head HD0 described above. During this time, as shown, fly height

controller 10FHC' controls demultiplexer 60 and voltage drive circuit 50<sub>0</sub> to issue initial state voltage IC to heat element resistor 30<sub>0</sub>.

[0061] According to this preferred embodiment of the invention, therefore, important advantages are provided in controlling the fly height of read/write head assemblies in hard disk drives. As described above relative to this exemplary embodiment, the current conducted by a heat element resistor at the head assembly may be separately controlled for read and write operations, and may be so controlled in a programmable manner. Overdrive and underdrive levels for the heat element resistor current in transitions between read and write operations are enabled, and can occur in substantially an automatic manner, through implementation of the preferred embodiment of the invention. In addition, if desired, an initial state drive level for the heat element resistor for unselected hard drives, and unselected read/write heads, is also provided. These advantages may be attained in an efficient manner, by way of relatively simple logic circuitry that may be implemented along with other functions, such as in a combined preamplifier and fly height controller integrated circuit.

[0062] The multi-channel implementation described above provides the additional benefits of providing separate fly height control in each of multiple read/write head assemblies, while minimizing the power dissipation and circuit complexity required for such control by sharing the control logic and digital-to-analog converters among the multiple heads. In this way, programmable fly height control current for read and write operations, automatic programmable overdrive and underdrive levels for in transitions between read and write operations, and the inclusion of initial state drive level for the heat element resistor in unselected read/write heads, are provided for multiple heads in an efficient and cost-effective manner.

[0063] While the present invention has been described according to its preferred embodiments, it is of course contemplated that modifications of, and alternatives to, these embodiments, such modifications and alternatives obtaining the advantages and benefits of this invention, will be apparent to those of ordinary skill in the art having

reference to this specification and its drawings. It is contemplated that such modifications and alternatives are within the scope of this invention as subsequently claimed herein.